Amendments to the Claims:

1. (Original) A method of using static timing analysis to extract implicit connectivity graph information comprising:

creating a unique clock waveform;

defining a clock domain for the clock waveform;

injecting the clock domain into a control node;

propagating the clock waveform from the control node to a transitively adjacent observation node; and

retrieving transitively adjacent control node information to determine path delay information from the control node to the transitively adjacent observation node based upon propagation of the clock waveform.

2. (Original) The method of claim 1 wherein:

the clock domain includes a rising edge clock domain and a falling edge clock domain; and

the path delay information includes information relating to the rising edge clock domain and the falling edge clock domain.

3. (Original) The method of claim 1 wherein:

the transitively adjacent observation node becomes a pseudo control node.

4. (Currently Amended) The method of claim 1 wherein:

the connectivity graph includes information of a path between the control node and the transitively adjacent observation node.

5. (Original) The method of claim 1 wherein:

the path between the control node and the transitively adjacent observation node is a direct path.

6. (Original) The method of claim 1 wherein:

the path between the control node and the transitively adjacent observation node includes combinational logic.

7. (Original) The method of claim 1 wherein:

the path between the control node and the transitively adjacent observation node includes a flop.

8. (Original) The method of claim 1 wherein:

the path delay information includes timing constraint information.

9. (Original) The method of claim 8 wherein:

the timing constraint information includes setup constraint timing constraint information.

10. (Original) The method of claim 8 wherein:

the timing constraint information includes hold constraint timing constraint information.

11. (Original) A system for using static timing analysis to extract implicit connectivity graph information comprising:

means for creating a unique clock waveform;

means for defining a clock domain for the clock waveform;

means for injecting the clock domain into a control node;

means for propagating the clock waveform from the control node to a transitively adjacent observation node; and

means for retrieving transitively adjacent control node information to determine path delay information from the control node to the transitively adjacent observation node based upon propagation of the clock waveform.

12. (Original) The system of claim 11 wherein:

the clock domain includes a rising edge clock domain and a falling edge clock domain; and

the path delay information includes information relating to the rising edge clock domain and the falling edge clock domain.

13. (Original) The system of claim 11 wherein:

the transitively adjacent observation node becomes a pseudo control node.

14. (Currently Amended) The system of claim 11 wherein:

the connectivity graph includes information of a path between the control node and the transitively adjacent observation node.

15. (Original) The system of claim 11 wherein:

the path between the control node and the transitively adjacent observation node is a direct path.

16. (Original) The system of claim 11 wherein:

the path between the control node and the transitively adjacent observation node includes combinational logic.

17. (Original) The system of claim 11 wherein:

the path between the control node and the transitively adjacent observation node includes a flop.

18. (Original) The system of claim 11 wherein:

the path delay information includes timing constraint information.

19. (Original) The system of claim 18 wherein:

the timing constraint information includes setup constraint timing constraint information.

20. (Original) The system of claim 18 wherein:

the timing constraint information includes hold constraint timing constraint information.

21. (Original) An apparatus for using static timing analysis to extract implicit connectivity graph information comprising:

a clock waveform module, the clock module creating a unique clock waveform;

a clock domain module, the clock domain module defining a clock domain for the clock waveform;

an injecting module, the injecting module injecting the clock domain into a control node;

a propagating module, the propagating module propagating the clock waveform from the control node to a transitively adjacent observation node; and

a retrieving module, the retrieving module retrieving transitively adjacent control node information to determine path delay information from the control node to the transitively adjacent observation node based upon propagation of the clock waveform.

22. (Original) The apparatus of claim 21 wherein:

the clock domain includes a rising edge clock domain and a falling edge clock domain; and

the path delay information includes information relating to the rising edge clock domain and the falling edge clock domain.

23. (Original) The apparatus of claim 21 wherein:

the transitively adjacent observation node becomes a pseudo control node.

24. (Currently Amended) The apparatus of claim 21 wherein:

the connectivity graph includes information of a path between the control node and the transitively adjacent observation node.

25. (Original) The apparatus of claim 21 wherein:

the path between the control node and the transitively adjacent observation node is a direct path.

26. (Original) The apparatus of claim 21 wherein:

the path between the control node and the transitively adjacent observation node includes combinational logic.

27. (Original) The apparatus of claim 21 wherein:

the path between the control node and the transitively adjacent observation node includes a flop.

28. (Original) The apparatus of claim 21 wherein:

the path delay information includes timing constraint information.

29. (Original) The apparatus of claim 28 wherein:

the timing constraint information includes setup constraint timing constraint information.

30. (Original) The apparatus of claim 28 wherein:

the timing constraint information includes hold constraint timing constraint information.